IN THE CLAIMS:

Kindly replace the claims of record with the following full set of claims:

1.- 4. (Cancelled)

5. (Currently amended) An arrangement for interference compensation in a phase-locked loop comprising:

a voltage-controlled frequency generator, ~~wherein the frequency generator has~~ having a V_{tune} input and a VarGND terminal, wherein ~~characterized in that~~ the VarGND terminal ~~for the voltage-controlled frequency generator (3)~~ is connected to a controllable voltage source comprising:

a resistor connected between the VarGND terminal and a GND potential of a loop filter of said phase-locked loop; and

a controllable current source connected between the VarGND terminal and the resistor.

6. (Cancelled)

7. (Currently amended) An arrangement as claimed in claim 5 [[6]], wherein ~~characterized in that~~ the VarGND terminal of ~~the voltage-controlled frequency generator (3)~~ is connected to a digital-to-analog converter ~~(5)~~ which generates a compensation current, and in that the digital-to-analog converter ~~(5)~~ is connected to two registers via a transmit/receive change-over switch.

8. (Currently amended) An arrangement as claimed in claim 5, wherein ~~characterized in that~~ the VarGND terminal is connected to the controllable voltage source via a voltage divider, wherein ~~in such a way that~~ the voltage divider is connected via a first partial resistor to the controllable voltage source, and [[the]] a second partial resistor, which is connected in series, is connected to the GND potential and the VarGND terminal with the connection to the first partial resistor is connected to the second partial resistor.

9. (Currently amended) An arrangement as claimed in claim 5, ~~characterized in that~~ a phase detector charge pump ~~(1)~~ is arranged to which a reference clock is applied via a first phase detector input (PDin1), wherein the output of the phase detector charge pump (Cpout) is connected to the input of a voltage-controlled frequency generator ~~(3)~~ via a loop filter ~~(2)~~, wherein the output of the voltage-controlled frequency generator ~~(3)~~ is connected to a second phase detector input (PDin2) via a frequency divider ~~(4)~~, ~~wherein, furthermore, a measuring circuit is arranged, and~~ wherein the loop filter ~~(2)~~ comprises a first capacitor at the input end, a third capacitor at the output end, a second resistor arranged between the input and the output of the loop filter and a series circuit which is connected to the input and comprises a first resistor and a second capacitor, wherein the second capacitor of the series circuit is connected to the input of the measuring circuit, while the input in the measuring circuit forms a virtual ground terminal.

10. (Currently amended) An arrangement as claimed in claim 9, ~~characterized in that~~ ~~the~~ further comprising:

a measuring circuit ~~comprises~~ comprising a negative-feedback inverting operational amplifier arrangement ~~(6)~~ and an analog-to-digital converter unit ~~(7)~~.

11. (Currently amended) An arrangement as claimed in claim 5, further comprising: ~~characterized in that~~ a measuring circuit [[is]] connected to the V_{tune} input of the voltage-controlled frequency generator ~~(3)~~, ~~that~~ the measuring circuit comprises:

a first operational amplifier which works as a buffer amplifier whose output is connected via a first resistor and a capacitor to [[the]] an inverting input of a second operational amplifier, working as a negative-feedback inverting amplifier, and ~~that the~~ a non-inverting input of the second operational amplifier [[is]] connected to a reference voltage, wherein ~~that~~ the output of the second operational amplifier is fed back to the inverting input via two anti-parallel diodes, and ~~that~~ the output of the second operational amplifier is further connected via a second resistor to the connection of the first resistor and the capacitor, and the output of the second operational amplifier has a TDet terminal for outputting a voltage.